

Abstract of the Disclosure

A flash memory device that has a global and local bit line design that enables an alternate bit line stress mode as well as a way to detect short circuits in local and global bit lines with a single alternate bit line program. The flash memory device has a plurality of sets of adjacent local bit lines, a plurality of global bit lines and a plurality of select transistors. Each select transistor has a control gate and is coupled between one of the local bit lines in each set of local bit lines and one of the global bit lines. Thus, each local bit line in each set of local bit lines is coupled to a different global bit line. Multiple select lines are used to activate the control gates on the select transistors. Each select line is coupled to the control gates on associated select transistors. The associated select transistors are select transistors that are coupled to the local bit lines in an associated set of local bit lines.

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